A 6 Watt Ka-Band MMIC Power Module Using MMIC Power Amplifiers

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Abstract

In this paper we present the development of a 6 Watt 24% PAE Ka-band power module with an associated power gain of 21.5 dB. The power module consists of a driver amplifier and two power amplifier chips. These MMIC amplifiers were fabricated with a 2-mil thick substrate using 0.15-µm InGaAs/AlGaAs/GaAs HEMT technology. The driver amplifier is a fully matched single-ended design with an output power of 27.5 dBm, a 10.7 dB power gain and 27% PAE. We use a hybrid approach for the output power amplifier which consists of two partially-matched MMIC chips and a 8-way Wilkinson combiner fabricated on Alumina substrate. The MMIC power amplifiers delivered a record power of 35.4 dBm (3.5W) with a PAE of 28% and an associated power gain of 11.5 dB. The 8-way combiner has an insertion loss of 0.6 dB. We believe this is a new benchmark for power module using monolithic approach at this frequency range.

Introduction

There has been numerous reports on the monolithic power amplifier performance [1] - [8]. The best power at Ka-band is about 1 W. This work benchmarks the state-of-the-art performance achieved by a single MMIC chip and a module using these chips as building blocks.

2-mil GaAs wafer offers the advantages of providing shorter thermal path and smaller via hole pattern to the back side, thus allowing multiple via holes to be inserted between gate fingers without increasing the pitch of the gate fingers. This multiple via holes to ground lowers the overall source inductance of the device. This will improve the gain and PAE of the amplifier especially at millimeter-wave frequency range. These multiple vias to ground also substantially improve the thermal dissipation of the heat generated per such small device area. Based on our past experience with 4-mil substrate designs, the power density delivered by 2-mil device is at least 25-35% better than the 4-mil device of similar periphery [1] - [4], [6] [7].

Design

Driver Amplifier

Fig. 1 shows the photo of the driver amplifier. The driver amlifier is a two-stage single-ended design with the output device periphery of 1.52 mm. Conservative device drive ratio was used to ensure enough power to drive the output stage over process variation. Harmonic terminations were provided at the drain to improve the PAE and these also help the out of band stability. This chip was fully matched to 50 ohm at the input and output. Stability analysis was done on both stages to make sure there was sufficient margin over process variation. Odd mode clamping resistors were inserted between FETs to suppress the push-pull oscillation. Odd mode stability analysis was done according to[10]. Out of band oscillation was suppressed by resistively loaded quarterwave stubs. The chip can be biased from either side for flexibility of insertion into different power modules. The chip area is 4.0x1.5 mm.

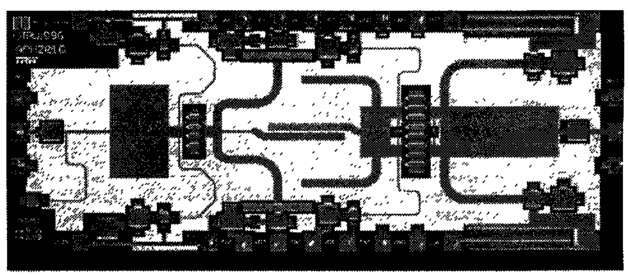

Figure 1. Photo of the driver amplifier MMIC chip (4.0x1.5mm)

Power Amplifier

Fig. 2 shows the photo of the power amplfier. The output MMIC power amplifier is a two-stage single-ended design with the output device periphery of 6.72mm. The optimum load at the fundamental and 2nd harmonic were determined from the computer load pull of the non-linear model. A wide transmission line was used to transform the device impedance to some non-50 ohm intermediate impedance. Odd mode clamping resistors were inserted between FETs to suppress the push-pull oscillation. Harmonic terminations were provided at the drain to improve the PAE and these also help the out of band stability. Out of band oscillation was suppressed by resistively loaded quarterwave stubs. Drain bias currents are provided through the off-chip 8-way combiner. The layout of the chip is completely symmetrical to suppress any odd mode oscillation and the biases can be provided from either side of the chip. Based upon the capability of the TRW automated assembly line, the statiscal average of the gap spacing was determined for the MMIC-MIC interface. This was simulated using a 3-D full-wave electromagnetic simulator, High Frequency System Simulator (HFSS) and the mismatch loss of the ribbon was compensated on the MIC side.

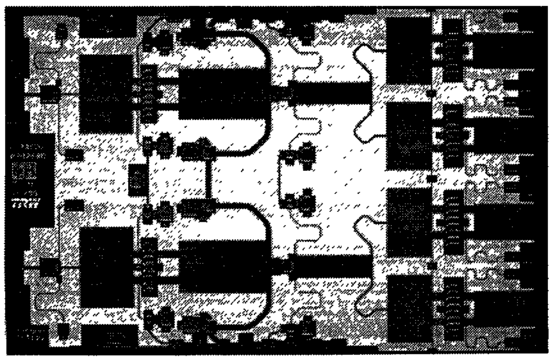

Figure 2. Photo of the power amplifier MMIC chip (4.8x3.1mm)

Wilkinson Combiners

The output 8-way off-chip combiner consists of three tiers of Wilkinson binary combiners in microstrip configuration. The impedance level of the microstrip lines was chosen such as to give a wide line width. Hence the dissipative transmission loss of the combiners was minimized.

Each Wilkinson combiner was designed separately to operate between the chosen port impedance. It was modelled on either Sonnet or HFSS and simulated in order to obtain the frequency response. The arm line of each combiner was then adjusted in length and width to obtain the best return loss and transmission loss. The combiner was fine tuned for best input port match and port-to-port isolation. Due to the close proximity of the input ports, the final configuration had a simulated transmission unbalance of 0.3 dB and 8 deg. A bias feed was also designed on the combiner substrate. It was a three section band stop filter. Its measured rejection at Ka-band was 35 dB.

The combiner was measured in a back-to-back configuration. The measured loss of one combiner was 0.6 dB

The input combiner consists of two levels of Wilkinson binary combiners and the measured loss of the combiner is 0.4 dB

Measured Performance

Fig. 3 shows the measured power, power gain and the PAE of the driver amplifierat 34.5 GHz. The PAE peaks at 27% with an output power of 27.5 dBm and an associated gain of 10.7 dB. Fig. 4 shows the in-fixture measured performance of the power amplifier at 34.5 GHz. The power amplifier demonstrated 35.4 dBm (3.5 W) at 28% PAE with an associated power gain of 11.5 dB. Fig. 5 shows a photo of the power module with one driver amplifier driving two power amplifiers. The 4-way splitter has a measured loss of 0.4 dB and the 8-way combiner at the output has a measured loss of 0.6 dB. Fig. 6 shows the measured performance of the entire power module including its coaxial interfaces (K-connectors) with an output power of 37.8 dBm (> 6 Watt) and PAE of 24% and an associated gain of 21.5 dB at 34.5 GHz.

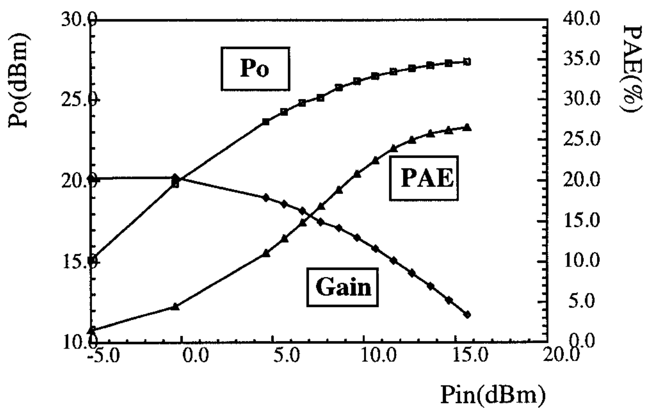

Figure 3. Chip performance for MMIC driver amplifier at 34.5 GHz

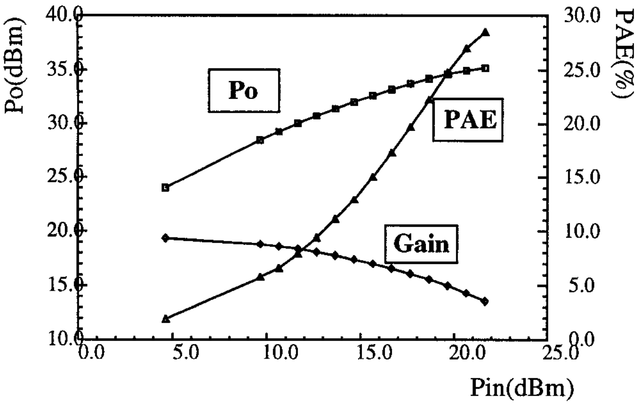

Figure 4. Chip performance for MMIC power amplifier at 34.5 GHz

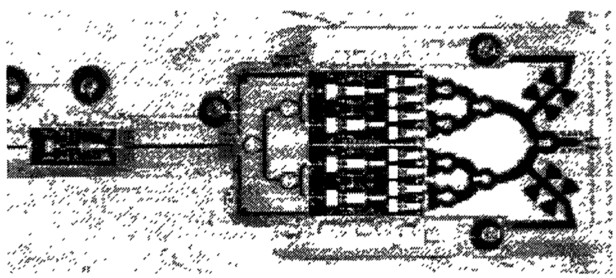

Figure 5. Photo of the 6 Watt power module

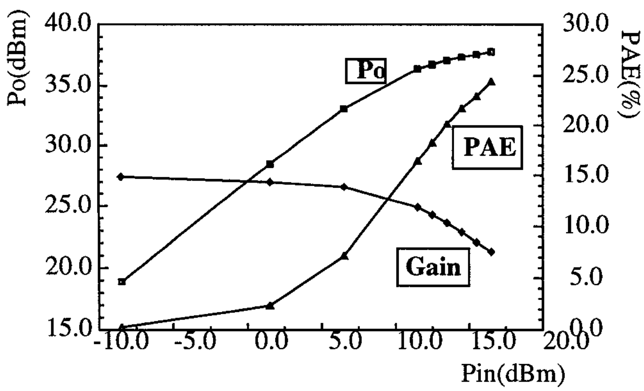

Figure 6. Measured in-fixture performance of the 6 Watt power module

Conclusion

We have demonstrated a 6 W, 24% PAE and 21.5 dB power gain Ka-band power module using 3 mmic chips. The MMIC power amplifier chip has achieved 3.5 W output power at 28% PAE with an associated power gain of 11.5 dB.

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